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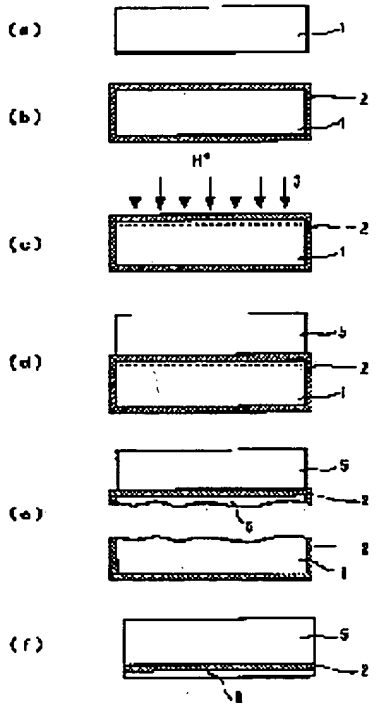
(54) SILICON WAFER MANUFACTURING METHOD AND SILICON WAFER

(57)Abstract:

PROBLEM TO BE SOLVED: To manufacture an SOI structured semiconductor wafer having no defective surface by a method wherein the surface whereon a silicon wafer that is the part laminated with a substrate member and then peeled is annealed in hydrogen atmosphere to be peeled is flattened.

SOLUTION: A silicon oxide film 2 is formed on the surface of a silicon wafer member 1 for implanting hydrogen ion on the surface of the film 2 to form a hydrogen implanted layer 4. Later, a substrate member 5 is laminated with the main surface of the silicon wafer member 1 and then the silicon wafer member 1 is heated so as to peel the surface part of the silicon wafer member 1 on the laminated side of the substrate member 5 from the hydrogen implanted layer 4 to manufacture a silicon wafer 6. Next, the silicon wafer 6 on the part of the laminated side with the substrate member 5 is annealed in hydrogen atmosphere to planarize the peeled surface. Through these procedures, the surface layer bearing excellent characteristics affected by no chemical mechanical polishing steps at all can be manufactured.



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CLAIMS

[Claim(s)]
[Claim 1] The process which pours in a hydrogen ion from the principal plane of 1 of the silicon wafer material by which silicon oxide was formed in the front face, and forms a hydrogen impregnation layer, The process which makes substrate material rival in above-mentioned silicon wafer material top Norikazu's principal plane, The process which strips the silicon wafer of a part which heats the above-mentioned silicon wafer material and was stretched with the above-mentioned substrate material of the above-mentioned silicon wafer material in the above-mentioned hydrogen impregnation layer, The manufacture approach of the silicon wafer characterized by including the process which makes flat the front face which annealed the above-mentioned silicon wafer of the part which stretched with the above-mentioned substrate material, was put together, and was removed in the hydrogen ambient atmosphere, and was removed.
[Claim 2] The manufacture approach of the silicon wafer according to claim 1 characterized by heating the above-mentioned annealing in the range of 1050-degree Centigrade to 1350 degrees, and performing it.
[Claim 3] The manufacture approach of the silicon wafer according to claim 1 characterized by performing the above-mentioned annealing by the plasma treatment in a hydrogen ambient atmosphere.
[Claim 4] The manufacture approach of the silicon wafer according to claim 1 characterized by performing the above-mentioned annealing by rapid thermal annealing.
[Claim 5] The manufacture approach of the silicon wafer according to claim 1 to 4 characterized by carrying out after performing chemical mechanical polish of the front face removed the account of a top in the above-mentioned annealing.
[Claim 6] The process which pours in a hydrogen ion from the principal plane of 1 of the silicon wafer material by which silicon oxide was formed in the front face, and forms a hydrogen impregnation layer, The process which makes substrate material rival in above-mentioned silicon wafer material top Norikazu's principal plane, The process which strips the silicon wafer of a part which heats the above-mentioned silicon wafer material and was stretched with the above-mentioned substrate material of the above-mentioned silicon wafer material in the above-mentioned hydrogen impregnation layer, The manufacture approach of the silicon wafer characterized by including the process which the front face of the above-mentioned silicon wafer of the part which stretched with the above-mentioned substrate material, was put together, and was removed is made to carry out epitaxial growth of the silicon, and forms a flat new front face in it.
[Claim 7] The manufacture approach of the silicon wafer according to claim 6 characterized by performing epitaxial growth of the above-mentioned silicon at the temperature of 800-degree more than Centigrade in trichlorosilan (SiHCl3), a dichloro silane (SiH2Cl2), a mono-KURORU silane (SiH2Cl), or a mono silane (SiH4).
[Claim 8] The silicon wafer characterized by being manufactured by the manufacture approach according to claim 1 to 7.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of the silicon wafer of SOI (Silicon on Insulator) structure effective in low-power-izing of a semiconductor device, improvement in the speed, and high integration.
[0002]
[Description of the Prior Art] Although various approaches are proposed as the manufacture approach of a SOI wafer from the former, the approach called the smart cutting method is in the approach made leading in recent years (for example, ELECTRONICS LETTERS 31 (1995) 1201 reference). If the smart cutting method is explained, a silicon wafer will be first oxidized thermally and silicon oxide will be formed in a front face. Next, from a silicon wafer front face, hydrogen ion impregnation is performed and a hydrogen impregnation layer is formed. Next, a base wafer is stuck on a side with the hydrogen impregnation layer of a silicon wafer. Next, this silicon wafer is heated and a silicon front face is removed from a hydrogen impregnation layer. In this way, a thin silicon layer is formed on substrate material. Since a thin silicon layer removes and very small unevenness is formed in a field at this time, a front face is ground chemically mechanically, is graduated and a SOI wafer is manufactured. It is reported that the effect of chemical mechanical polish appears greatly in the property of a device and the yield on the other hand recently (H. Yamamoto et al, Proceeding of The 2 nd International Symposium on Advanced Science and Technology of Silicon Materials, P(1996) 425).
[0003]
[Problem(s) to be Solved by the Invention] The defect in polish of such a silicon wafer front face produced similarly the wafer of the SOI structure manufactured by the conventional approaches, such as the above smart cutting methods, and had become the cause of reducing the property of a device, and the yield. This invention tends to solve such a conventional problem and tends to offer the semiconductor wafer of the SOI structure which does not have a defect in a front face.
[0004]
[Means for Solving the Problem] The process which the manufacture approach of the silicon wafer this invention pours in a hydrogen ion from the principal plane of 1 of the silicon wafer material by which silicon oxide was formed in the front face, and forms a hydrogen impregnation layer, The process which makes substrate material rival in above-mentioned silicon wafer material top Norikazu's principal plane, The process which strips the silicon wafer of a part which heats the above-mentioned silicon wafer material and was stretched with the above-mentioned substrate material of the above-mentioned silicon wafer material in the above-mentioned hydrogen impregnation layer, It is characterized by including the process which makes flat the front face which annealed the above-mentioned silicon wafer of the part which stretched with the above-mentioned substrate material, was put together, and was removed in the hydrogen ambient atmosphere, and was removed.
[0005] Moreover, the manufacture approach of the silicon wafer this invention is characterized by heating the above-mentioned annealing in the range of 1050-degree Centigrade to 1350 degrees, and

performing it. Moreover, the manufacture approach of the silicon wafer this invention is characterized by performing the above-mentioned annealing by the plasma treatment in a hydrogen ambient atmosphere.
[0006] Moreover, the manufacture approach of the silicon wafer this invention is characterized by performing the above-mentioned annealing by rapid thermal annealing. Moreover, the manufacture approach of the silicon wafer this invention is characterized for the above-mentioned annealing by carrying out, after performing chemical mechanical polish of the removed front face the account of a top.
[0007] Moreover, the manufacture approach of the silicon wafer this invention The process which pours in a hydrogen ion from the principal plane of 1 of the silicon wafer material by which silicon oxide was formed in the front face, and forms a hydrogen impregnation layer, The process which makes substrate material rival in above-mentioned silicon wafer material top Norikazu's principal plane, The process which strips the silicon wafer of a part which heats the above-mentioned silicon wafer material and was stretched with the above-mentioned substrate material of the above-mentioned silicon wafer material in the above-mentioned hydrogen impregnation layer, It is characterized by including the process which the front face of the above-mentioned silicon wafer of the part which stretched with the above-mentioned substrate material, was put together, and was removed is made to carry out epitaxial growth of the silicon, and forms a flat new front face in it. Moreover, the manufacture approach of the silicon wafer this invention is characterized by performing epitaxial growth of the above-mentioned silicon at the temperature of 800-degree more than Centigrade in trichlorosilan (SiHCl3), a dichloro silane (SiH2Cl2), a mono-KURORU silane (SiH2Cl), or a mono silane (SiH4).
[0008]
[Embodiment of the Invention] Hereafter, the gestalt of implementation of this invention is explained with reference to drawing. In addition, the same sign shows a same or considerable part among drawing.

Gestalt 1. drawing 1 of operation is drawing explaining the manufacture approach of the SOI wafer of the gestalt 1 implementation this invention, and (a) - (f) shows the sectional view of each process. If this manufacture approach is explained, as are first shown in drawing 1 (a), and the silicon wafer material 1 is prepared and it is shown in drawing 2 (b), the silicon wafer material 1 will be oxidized thermally and silicon oxide 2 will be formed in a front face. Next, as shown in drawing 1 (c), from one front face of the silicon wafer material 1, hydrogen ion impregnation of 2x1016 - 1x1017-/cm2 is performed, and the hydrogen impregnation layer 4 is formed. Then, as shown in drawing 1 (d), the substrate material 5 with another, suitable silicon wafer material (base wafer) etc. for the front-face side which carried out hydrogen impregnation of the silicon wafer material 1 is stuck.
[0009] Then, if this silicon wafer material 1 is heated at 400-600 degrees C, as shown in drawing 5 (e), the surface part of the silicon wafer material 1 of the side by which the substrate material 5 was stretched can be removed from the hydrogen impregnation layer 4. In this way, the silicon wafer 7 of the SOI structure in which the thin silicon layer 6 was formed on the substrate material 5 is obtained. At this time, the thin silicon layer 6 removes and unevenness of about 20nm is formed in a field. Therefore, if needed, as shown in drawing 5 (f), the front face of the silicon layer 6 is ground chemically mechanically, and is graduated. The process so far is the same as that of the approach called the so-called smart cutting method.
[0010] Next, the silicon wafer 7 is annealed in a hydrogen ambient atmosphere. Drawing 2 wets the annealer (furnace) for performing annealing. In drawing 2 , the silicon wafer with which 7 carries out annealing, the holder with which 8 holds this wafer, and 9 are furnace bodies. Hydrogen gas is introduced from the up entry of a furnace body 9, and it is discharged from a lower outlet. This annealing furnace performs annealing for several 10 seconds to several 10 minutes for the silicon wafer 7 of the phase of drawing 1 (e) in a hydrogen ambient atmosphere at 1350 degrees from 1050-degree Centigrade. The silicon wafer 7 with a flat front face as this shows to drawing 1 (f) is obtained. If heating temperature is 1050-degree less than Centigrade, annealing will take long duration to it. Moreover, if heating temperature is 1350-degree more than Centigrade, since silicon will fuse, it is not

suitable. Thus, stabilization of a process, improvement in a throughput, and improvement in wafer quality are realizable by making heating temperature into the range of 1050-degree Centigrade - 1350 degrees.

[0011] By annealing in the inside of a hydrogen ambient atmosphere, a surface silicon atom depends on effectiveness [that the front face of a silicon wafer becomes flat], such as carrying out a rearrangement, as mentioned above. The situation of the rearrangement of a silicon atom is shown in drawing 3 . Drawing 3 (a) is the sectional view in which having expanded the silicon front face before annealing, and having shown it typically. If it heats in a hydrogen ambient atmosphere, as shown in drawing 3 (b), a silicon front face is activated by the effectiveness of hydrogen, and a silicon atom will move a front face and will move to the point stabilized [time rate energy]. Consequently, a front face becomes flat as shown in drawing 3 (c).

[0012] If the silicon wafer which anneals is annealed while the front face had separated in the phase of drawing 1 (e), it can manufacture a silicon wafer without the effect of chemical mechanical polish. Moreover, in the phase of drawing 1 (f), before annealing, chemical mechanical polish may be moderately given to extent which does not leave effect to a front face if needed. When moderate chemical mechanical polish is given beforehand, the silicon wafer which can attain simplification of annealing by hydrogen and speeding up, and finally does not have the effect of chemical mechanical polish also in this case can be obtained.

[0013] Gestalt 2. drawing 4 of operation is drawing explaining the manufacture approach of the silicon wafer of the SOI structure of the gestalt 2 implementation this invention, and shows a rapid annealer. In drawing 4 , the silicon wafer with which 7 carries out annealing, the holder (susceptor) with which 10 holds this silicon wafer, and 11 show lamps, such as a transparence chamber and infrared radiation for heating in 12. Hydrogen gas is introduced from the inlet port on the left-hand side of [illustration] a chamber 11, and is discharged from a right-hand side outlet.

[0014] With the gestalt 1 of operation, the batch method which used the annealing furnace is performing hydrogen processing. With the gestalt of this operation, the processing of a sheet for every one silicon wafer is possible, and it processes by the so-called short-time annealing (rapid thermal annealing) which carries out a short-time exposure and anneals thermal radiation light to a silicon wafer. As a rapid annealer, a FURASHU lamp annealer with the infrared annealer by the halogen lamp, an arc lamp, etc., a xenon FURASHU lamp, etc. is used. In addition, the preparation process of the silicon wafer 7 of annealing is the same as the gestalt 1 of operation. According to such short-time annealing, there is effectiveness of being easy to control a process.

[0015] Gestalt 3. drawing 5 of operation is drawing explaining the manufacture approach of the silicon wafer of the SOI structure of the gestalt 3 implementation this invention, and shows a plasma annealer. In drawing 5 , in the silicon wafer with which 7 carries out annealing, the electrode with which 13 sandwiches the silicon wafer 7, and 14, a chamber and 15 show a high frequency generating machine, and 16 shows a capacitor. Moreover, the bottom electrode of an electrode 13 controls temperature at several 100 degrees C with the heating apparatus which is not illustrated. Hydrogen gas is introduced from the inlet port on the left-hand side of [illustration] a chamber 14, and is discharged from a right-hand side outlet. In this example, high-frequency power is performing plasma treatment in hydrogen. Moreover, generating of the plasma may be performed using other sources of excitation, such as ECR (electron cyclotron resonance) and light. In addition, the preparation process of the silicon wafer 7 of annealing is the same as the gestalt 1 of operation.

[0016] The gestalten 1 and 2 of operation are performing by annealing in high temperature processing in hydrogen. With the gestalt of this operation, hydrogen processing is carried out in the plasma and annealing is performed. When it does in this way, there is effectiveness of being able to lower processing temperature from a room temperature to about 600 degrees C. Moreover, in such plasma treatment, since the processing time is short compared with the gestalt 1 of operation, it has the effectiveness of that it is easy to control a process, contamination being hard to be introduced.

[0017] Gestalt 4. drawing 6 of operation is drawing explaining the manufacture approach of the silicon wafer of the SOI structure of the gestalt 4 implementation this invention, and shows the epitaxial growth

system of silicon. In drawing 6 , the silicon wafer to which 7 carries out epitaxial growth, the holder which 17 holds this silicon wafer and rotates, and 18 show a high frequency coil, and 19 shows a chamber. Hydrogen gas is introduced from the inlet port on the left-hand side of [illustration] a chamber 14, and is discharged from a right-hand side outlet.

[0018] With the gestalt 1 of operation, wafer ** is performing hydrogen annealing after **. On the other hand, with the gestalt of this operation, after removing the thin silicon layer 6 from the hydrogen impregnation layer 4 at the process of drawing 1 (e), epitaxial growth of silicon is carried out to the removed field, and a new front face is evenly formed in it. Epitaxial growth of this silicon is performed above 800 degrees C in trichlorosilan (SiHCl3), a dichloro silane (SiH2Cl2), a mono-KURORU silane (SiH2Cl), or a mono silane (SiH4). By using these ingredients, the defective reduction layer in the front face of a silicon growth phase can be formed. In addition, the preparation process of the silicon wafer 7 for carrying out epitaxial growth is the same as the gestalt 1 of operation. According to such a manufacture approach, when the effect of chemical mechanical polish can be lost, control of the thickness of the silicon layer 6 of a silicon wafer etc. is still attained.

[0019]

[Effect of the Invention] As explained above, according to this invention, the silicon wafer of SOI structure with which the front face was equipped with the surface layer with the sufficient property of not being influenced of chemical mechanical polish can be obtained.

[Translation done.]